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Claims

[c1] What is claimed is:

1.A method for forming a thin film transistor (TFT) of an organic light emitting display (OLED), the method comprising the steps of:

providing a substrate;

depositing a first metal layer on the substrate;

performing a first photo-etching-process (PEP) to remove a portion of the first metal layer to form a gate of the TFT on the surface of the substrate;

forming a gate insulating layer on the gate;

forming a microcrystalline silicon layer on the gate insulation layer;

forming an amorphous silicon layer on the microcrystalline silicon layer;

forming a doped n+ layer on the amorphous silicon layer;

performing a second PEP to remove a portion of the doped n+ layer, the amorphous silicon layer, and the microcrystalline silicon layer;

forming a second metal layer on the substrate;

performing a third PEP to form a source and a drain of the TFT on the surface of the substrate, and simultane-

ously to remove a portion of the doped n+ layer to expose the amorphous silicon layer; and
forming a passivation layer on the substrate.

[c2] 2.The method of claim 1, wherein the substrate is selected from the group consisting of a glass substrate, a quartz substrate, and a plastic substrate.

[c3] 3.The method of claim 1, wherein the first metal layer and the second metal layer are composed of tungsten (W), chromium (Cr), aluminum (Al), copper (Cu), molybdenum (Mo),or an alloy of any of the above metals.

[c4] 4.The method of claim 1, wherein the gate insulating layer is formed with a plasma enhanced chemical vapor deposition (PECVD) process, the gate insulating layer comprising silicon oxide (SiO_x), silicon nitride (SiN_y), or silicon oxynitride (SiON).

[c5] 5.The method of claim 1, further comprising the step of performing a nitrous oxide (N_2O) plasma process for treating the surface of the gate insolating layer.

[c6] 6.The method of claim 1, further comprising the step of performing an oxygen-containing plasma process for treating the surface of the gate insulating layer.

[c7] 7.The method of claim 6, wherein an oxygen-containing

gas of the oxygen-containing plasma process comprises nitric oxide (NO_x), hydrogen peroxide (H_2O_2), oxygen (O_2), ozone (O_3), or tetra-ethyl-ortho-silicate (TEOS).

[c8] 8.The method of claim 1, wherein the microcrystalline silicon layer is formed with a PECVD process, and the power density of the PECVD process is less than 0.54 w/cm^2.

[c9] 9.The method of claim 8, wherein a thickness of the microcrystalline silicon layer is approximately 50 to 500 angstroms (Å), and a crystallization ratio (f_c) of the microcrystalline silicon layer is more than 40%.

[c10] 10.The method of claim 1, wherein the gate insulating layer, the microcrystalline silicon layer, and the amorphous silicon layer are formed by a same PECVD process with continuous deposition.

[c11] 11.The method of claim 1, wherein the gate insulating layer and the microcrystalline silicon layer are deposited by a PECVD process with interrupted deposition.

[c12] 12.The method of claim 1, wherein the passivation layer comprises silicon oxide or silicon nitride.

[c13] 13.A method for forming a TFT of an OLED, the method comprising the steps of:

providing a substrate;
depositing a first metal layer on the substrate;
performing a first PEP to remove a portion of the first metal layer to form a gate of the TFT on the surface of the substrate;
forming a gate insulating layer on the gate;
performing a surface treatment to the surface of the gate insulating layer;
forming a microcrystalline silicon layer on the gate insulating layer;
forming an amorphous silicon layer on the microcrystalline silicon layer;
forming a doped n+ layer on the amorphous silicon layer;
performing a second PEP to remove a portion of the doped n+ layer, the amorphous silicon layer, and the microcrystalline silicon layer;
forming a second metal layer on the substrate;
performing a third PEP to form a source and a drain of the TFT on the surface of the substrate, and simultaneously to remove a portion of the doped n+ layer for exposing the amorphous silicon layer; and
forming a passivation layer on the substrate.

[c14] 14.The method of claim 13, wherein the surface treatment is a nitrous oxide (N_2O) plasma process.

[c15] 15.The method of claim 13, wherein the surface treatment is an oxygen-containing plasma process.

[c16] 16.The method of claim 15, wherein an oxygen-containing gas of the oxygen-containing plasma process comprises nitric oxide (NO_x), hydrogen peroxide (H_2O_2), oxygen (O_2), ozone (O_3), or tetra-ethyl-ortho-silicate (TEOS).

[c17] 17.The method of claim 13, wherein the substrate is selected from the group consisting of a glass substrate, a quartz substrate, and a plastic substrate.

[c18] 18.The method of claim 13, wherein the first metal layer and the second metal layer are composed of tungsten, chromium, aluminum, copper, molybdenum, or an alloy of any of the above metals.

[c19] 19.The method of claim 13, wherein the gate insulating layer is formed with a PECVD process, and the gate insulating layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

[c20] 20.The method of claim 13, wherein the microcrystalline silicon layer is formed by a PECVD process, and a power density of the PECVD process is less than 0.54 w/cm^2.

[c21] 21.The method of claim 20, wherein a thickness of the

microcrystalline silicon layer is approximately 50 to 500 angstroms (Å), and a crystallization ratio (f_c) of the microcrystalline silicon layer is more than 40%.

[c22] 22.The method of claim 13, wherein the gate insulating layer, the microcrystalline silicon layer, and the amorphous silicon layer are formed by a same PECVD process with continuous deposition.

[c23] 23.The method of claim 13, wherein the gate insulating layer and the microcrystalline silicon layer are formed by a PECVD process with interrupted deposition.

[c24] 24.The method of claim 13, wherein the passivation layercomprises silicon oxide or silicon nitride.